[*INTEGRATED CIRCUIT PACKAGE AND METHOD OF MANUFACTURE*]

Abstract of Disclosure

An integrated circuit package and a method of manufacturing the package. A silicon chip is attached to the surface of a substrate or attached to the bottom surface of a cavity in the substrate so that the active surface of the chip is exposed. One or more build-up circuit structures are formed over the substrate. Each build-up circuit structure has at least one insulation layer, at least one patterned circuit layer and a plurality of via openings with conductive material therein so that bonding pads on the active surface of the chip connect electrically with the patterned circuit layer through the vias. To form a ball grid array package, solder balls may also be attached to the solder ball pads on the patterned circuit layer so that the bonding pads on the chip are electrically connected to an external circuit through the build-up circuit structure and the solder balls.

Figures